

ABSTRACT OF THE DISCLOSURE

Specified thin-film transistors 26 and 27 are caused to conduct by a gradation signal inputted in control circuits 24 and 25, and resistors with a conduction resistance of activated transistors are inserted between any of reference voltages V0, V2, and V4 and an output terminal T1 or between any of reference voltages V1 and V3 and an output terminal T2, and a pair of thin-film transistors 29 in a sampling circuit 23 are caused to conduct simultaneously in sync with the gradation signal. If a signal line SL1 is selected, reference voltages V0, V2, or V4 and V1 or V3 are applied to the signal line SL1, either as they are or as divided by the conduction resistance of the activated thin-film transistors, by using a junction point between the sampling circuit 23 and signal line SL1 as a voltage dividing point.

2025 RELEASE UNDER E.O. 14176